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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,071	06/25/2003	Stanislav Peter Bajuk	BUR920030051US1	1070

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EXAMINER	
TO, TUYEN P	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,071	BAJUK ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *22 and 23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21* is/are rejected.

7)☒ Claim(s) *1-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 06/25/2003. Claims 1-23 are pending.

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

Group I, Claim(s) 1-21, drawn to a method for creating a logic design with signal interconnect types and language extensions, classified in class 716, subclass 16.

Group II, Claim(s) 22-23, drawn to an array/set of placeable tiles with a same/different outline size but a different amount of FPGA and standard cell logic, classified in class 326, subclass 41.

2. The inventions are distinct, each from the other because of the following reasons:

Invention group I and group II are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01). In the instant case the different invention group I is directed toward a creation of a heterogeneous integrated circuit device through synthesis using RTL. The invention group II is directed toward the arrangement of programmable logic and standard cell logic in an integrated circuit.

3. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with **Anthony P. Ng. (Reg. No. 43,427)** on 12/12/2005 a provisional election was made **with traverse** to prosecute the invention of **Group I, claims 1-21**. Affirmation of this election must be made by applicant in replying to this Office action. Claims 22-23 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Specification

6. The disclosure is objected to because of the following informalities: in the abstract and on page 4, ll. 5; the phrase " the signal interconnect"s type" appears to be an error. It should be replaced with " the signal interconnect's type". On page 2, ll. 17 and 24, and on page 3, ll. 19, the " FPGA"s " , "OR"s" , "XOR"s", and " RTL"s" appear to be errors. They should be replaced with " FPGA's " , "OR's" , "XOR's", and " RTL's". Appropriate correction is required.

Claim Objections

7. **Claims 6, 13, and 19** are objected to because the recited "is capable of " is not a definite claim language. Appropriate correction is required.

8. **Claims 1, 9, and 16** are objected to because the recited " the signal interconnect"s type" appears to be an error. Appropriate correction is required.

9. **Claim 8** is objected to because the recited " repeated changing the signal interconnect type from a standard cell type to an FPGA type to make a more flexible logic" is not clearly described. Examiner suggests it to be changed to " repeatedly changing the signal interconnect type from a standard cell type to an FPGA type to create a flexible logic design". Appropriate correction is required.

10. **Claim 15** is objected to because the recited " means for repeatedly changing the signal interconnect type from a standard cell type to an FPGA type to make a logic more flexible" is not clearly described. Examiner suggests it to be changed to " means for repeatedly changing the signal interconnect type from a standard cell type to an FPGA type to create a flexible logic design". Appropriate correction is required.

Claim Rejections - 35 USC § 102/103

11. **Claim 21** is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Taguchi (US Pub. 2002/0066956).

Taguchi discloses a single placeable logic tile comprising:

a first portion containing a field programmable gate array (FPGA) logic (Fig. 1A-1B and 3A-3C; page2 [0026] through page 3 [0028]); and

a second portion containing a standard cell logic (Fig. 1A-1B and 3A-3C; page2 [0026] through page 3 [0028]), wherein the first portion and the second portion are synthesized from a single register transfer language (RTL) file having both FPGA and standard cell files (Taguchi discloses the hybrid integrated circuit (or the "logic tile") which comprises: "a common substrate on which an electrode pattern is formed; a first monolithic semiconductor chip designed by the used of an ASIC technology and

mounted on the common substrate; a second monolithic semiconductor chip designed by the use of an FPGA technology and mounted on the common substrate." see the abstract; page 2 [0026]).

12. The following is quoted from the MPEP (see page 2100-58, Product-by-process Claims [R-1]):

"[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process."

Allowable Subject Matter

13. **Claims 1-20** contain allowable subject matter.

The following is a statement of reasons for the indication of allowable subject matter: in a method for creating a logic design using a register transfer language, *the prior art of record does not teach or fairly suggest* upon a declaration of a signal interconnect, defining a language extension of a register transfer language for the signal interconnect based on the signal interconnect"s type; storing different signal interconnect types in a same design file; and creating a logic design by partitioning between different types of cells in the logic design, wherein the different types of cells are based on the different signal interconnect types as described by the language extensions.

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272- 7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To

Patent Examiner

AU 2825

A. M. Thompson
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Technology Center Z800